REMARKS

The application has been carefully reviewed in light of the Final Office Action dated May 27, 2001 (Paper No. 7). Claims 1, 8, 9, 11, 14-16, 20-21, 23, 26, 33 and 34 have been amended to more clearly define the patentable subject matter of the invention. Claim 87 has been amended to correct a typographical error. Claims 38-46 and 48-55 have been allowed. Claims 1-37, 47, 56 and 82-98 are now pending in this case.

Claims 13, 15-16, 25, 37, 47 and 56 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Examiner notes that Claims 15-16 fail to particularly point out and distinctly claim the subject matter which Applicant regards as the invention because there are no transistors connected in parallel in Figure 2 or Figure 3. Claims 15-16 have been amended to remove the phrase "in parallel" and are now in condition for allowance.

The Examiner also notes that Claims 13, 25, 37, 47 and 56 fail to particularly point out and distinctly claim the subject matter which Applicant regards as the invention because there are no transistors connected in parallel in Figure 2 or Figure 3. Claim 13 recites "a third driver inverter connected in parallel to said first and second driver inverters." Similarly, Claims 25, 37, 47 and 56 refer to a third driver inverter connected in parallel. Applicant requests that the Examiner note that, in Fig. 5, driver inverter 78 is connected in parallel with driver inverters 72 and 74.

Claims 1-3, 6-8, 14-17, 19-20, 26-33, 36, 82-86 and 91-94 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Houston et al., U.S. Patent No. 6,037,808 (hereinafter "Houston"). The rejection is respectfully traversed.

The present invention is an apparatus and method for adjusting clock skew. To reduce the clock skew, a non-inverted clock signal ("CLK") and an inverted clock signal ("XCLK") are connected to back-to-back inverters. The signal that takes longer to switch states has an extra inverter driving it when it switches states and the signal that switches states faster has an extra inverter fighting it when it switches states so that the resulting output signals are in the same state for a shorter period of time and the clock skew is reduced. When the input signals CLK and XCLK are not switching and are in opposite states, this circuit does not affect the output signals.

Houston, however, is a circuit which senses data signals output from a memory array. Unlike the present invention which receives two complementary clock signals as inputs and adjusts them to reduce the skew between them, Houston uses differential silicon-on-insulator ("SOI") amplifiers having tied floating body connections to sense and amplify the difference between two data signals and outputs that signal and its complement on two output lines. Figure 10, cited by the examiner, uses the output lines DOUT and /DOUT to amplify a differential signal.

Claims 1, 8, 14-16, 20, 26 and 33 have been amended to recite input/output lines that receive and output complementary clock signals. Houston does not receive complementary clock signals as input signals or output complementary clocks signals.

Amended Claim 1 recites "at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals." If clock signals were input into the circuit recited in Houston, the skew of the signals would not be reduced. Instead, the output would be an amplification of the difference between the two input signals. Houston, therefore, does not recite all of the elements of amended Claim 1. Accordingly, amended Claim 1 is now in condition for allowance.

Claims 2-3 and 6-7 depend from amended Claim 1. For at least the reasons discussed above in reference to amended Claim 1, Claims 2-3 and 6-7are allowable along with amended Claim 1.

Amended Claim 8 recites "first and second input buffer circuits for receiving first and second external complementary clock signals." Accordingly, for at least the reasons discussed above in reference to amended Claim 1, Claim 8 is also patentable over Houston.

Amended Claim 14 recites "the respective connection terminal of said series connected complimentary transistors being coupled to respective of said complementary clock signal input/output lines." Amended Claim 14, like amended Claim 1, now recites complementary clock signal input/output lines." Accordingly, for at least the reasons discussed above in reference to amended Claim 1, Claim 14 is also patentable over Houston.

Amended Claim 15 depends from amended Claim 14 and is allowable for the reasons discussed above with reference to amended Claim 14.

Amended Claim 16 recites "at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second internal complementary clock signals." Amended Claim 16, like amended Claim 1, now recites receiving and outputting complementary clock signals. Accordingly, for at least the reasons discussed above with reference to amended Claim 1, amended Claim 16 is patentable over Houston.

Claims 17 and 19 depend from amended Claim 16 and are allowable for the reasons discussed above in reference to amended Claim 16.

Amended Claim 20 recites "first and second input buffer circuits for receiving first and second external complementary clock signals." Amended Claim 20, like amended Claim 16, now recites complementary clock signals. Accordingly, for at least the reasons discussed above in reference to amended Claim 16, amended Claim 20 is also patentable over Houston.

Amended Claim 26 recites "at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals." Amended Claim 26, like amended Claim 1, now recites complementary clock signals. Accordingly, for at least the reasons discussed above in reference to amended Claim 1, amended Claim 26 is also patentable over Houston.

Claims 27-32 depend from amended Claim 26 and are allowable for the reasons discussed above in reference to amended Claim 26.

Amended Claim 33 recites "first and second input buffer circuits for receiving first and second external complementary clock signals." Amended Claim 33, like amended Claim 26, now recites complementary clock signals. Accordingly, for at least the reasons discussed above in reference to amended Claim 26, amended Claim 33 is also patentable over Houston.

Claims 36 depends from amended Claim 26 and is allowable for the reasons discussed above in reference to amended Claim 26.

Claim 82 recites "receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal." Complementary signals, by definition, are the inverse of each other. Thus, Claim 82, like amended Claim 1, recites complementary clock signals. Accordingly, for at least the reasons discussed above in reference to amended Claim 1, Claim 82 is also patentable over Houston.

Claims 83-86 depend from Claim 82 and are allowable for the reasons discussed above in reference to Claim 82.

Claim 91 recites "receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal." Complementary signals, by definition, are the inverse of each other. Thus, Claim 91, like amended Claim 1, recites complementary clock signals. Accordingly, for at least the reasons discussed above in reference to amended Claim 1, Claim 91 is in condition for allowance.

Claims 92-94 depend from Claim 82. For at least the reasons discussed above in reference to Claim 91, Claim 92-94 are allowable along with Claim 91.

Claims 4-5 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Houston. The rejection is respectfully traversed.

Claims 4-5 depend from amended Claim 1. Therefore, Claims 4-5 now include the same limitations as amended Claim 1. For at least the reasons discussed above in reference to amended Claim 1, Claims 4-5 are allowable along with amended Claim 1.

Claims 12-13 and 36-37 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Oh, U.S. Patent No. 5,838,173 (hereinafter "Oh"), in view of Garcia, U.S. Patent No. 5,949,259 (hereinafter "Garcia").

Oh is a device and method for detecting a low voltage in a system. The latch 27 has an input B. The output of the latch 27 goes to C, the input to an inverter 28.

Claims 12-13 depend from amended Claim 1. Amended Claim 1 now recites "at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals." Oh, however, recites a circuit for detecting a low voltage in a system. The circuit described in Oh does not receive as inputs or output complementary clock signals. Garcia is likewise deficient. For at least the foregoing reasons, Claims 12-13 are patentable over Oh in view of Garcia.

Claims 36-37 depend from amended Claim 26. Amended Claim 26 recites "at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals." Again, neither Oh nor Garcial disclose these limitations. For at least these reasons, Claims 36-37 are patentable over Oh in view of Garcia.

Claims 18, 23-25, 87-90 and 95-98 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Houston in view of Oh and further in view of Garcia. The rejection is respectfully traversed.

Claims 18 and 24-25 depend from amended Claim 16. Amended Claim 16 recites "at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second internal complementary clock signals." As noted earlier, not one of Houston, Oh or Garcia teach or suggest these features. For at least these reasons, Claims 18 and 24-25 are patentable over Houston in view of Oh and further in view of Garcia.

Amended Claim 23 recites "a first and second driver circuit for boosting said output clock signal, said first and second driver circuit connected to said first and second complementary clock signal input/output lines, respectively." Amended Claim 23, like amended Claim 16, now recites complementary clock signals. Note one of Houston, Oh or Garcia teach or suggest these features. For at least these reasons, amended Claim 23 is patentable over Houston in view of Oh and further in view of Garcia.

Claims 87-90 depend from claim 82. As discussed above, Claim 82 recites "receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal." Not one of Houston, Oh or Garcia teach or suggest these features. Accordingly, for at least these reasons, Claims 87-90 are now in condition for allowance.

Claims 95-98 depend from claim 91. As discussed above, Claim 91 recites "receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal." Not one of Houston, Oh or Garcia teach or suggest these features. Accordingly, for at least these reasons, Claims 95-98 are patentable over Houston in view of Oh and further in view of Garcia.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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APPENDIX A

Version With Markings to Show Changes Made

1. (Amended) A circuit for reducing clock signal skew comprising:

at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals;

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second clock signal input/output line.

8. (Amended) The circuit of claim 1, further comprising first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line.

9. (Twice Amended) The circuit of claim 8, wherein each of said first and second input buffer circuits comprises:

an input for receiving one of said first and second external complementary clock signals;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said inputs, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second, complementary internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

11. (Amended) The circuit of claim 1, further comprising a first and second driver circuit [for boosting said output signal], said first and second driver circuit connected to said first and second complementary clock signal input/output lines, respectively.

14. (Amended) The circuit of claim 1, wherein each of said first and second inverters are comprised of series connected complimentary transistors, the respective connection terminal of said series connected complimentary transistors being coupled to a respective one of said complementary clock signal input/output lines.

15. (Amended) The circuit of claim 14, wherein said first and second inverters include:

a first N-channel transistor coupled [in parallel] to a second N-channel transistor, a gate of said first N-channel transistor coupled to receive said second clock

input signal, and said second N-channel transistor coupled to receive said first clock input signal;

a first P-channel transistor coupled [in parallel] to a second P-channel transistor, a gate of said first P-channel transistor coupled to receive said second clock input signal, and said second P-channel transistor coupled to receive said first clock input signal;

said second N-channel transistor coupled in series to said second P-channel transistor and said first clock signal input/output line connected between said second N-channel transistor and said second P-channel transistor; and

said first N-channel transistor coupled in series to said first P-channel transistor and said second clock signal input/output line connected between said first N-channel transistor and said first P-channel transistor.

16. (Amended) A circuit for reducing clock signal skew comprising:

at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second internal complementary clock signals;

a first N-channel transistor coupled [in parallel] to a second N-channel transistor, a gate of said first N-channel transistor coupled to receive said second clock input signal, and said second N-channel transistor coupled to receive said first clock input signal;

a first P-channel transistor coupled [in parallel] to a second P-channel transistor, a gate of said first P-channel transistor coupled to receive said second clock input signal, and said second P-channel transistor coupled to receive said first clock input signal;

said second N-channel transistor coupled in series to said second P-channel transistor and said first clock signal input/output line connected between said second N-channel transistor and said second P-channel transistor; and

said first N-channel transistor coupled in series to said first P-channel transistor and said second clock signal input/output line connected between said first N-channel transistor and said first P-channel transistor.

20. (Amended) The circuit of claim 16, further comprising first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line.

21. (Twice Amended) The circuit of claim 20, wherein each of said first and second input buffer circuits comprises:

an input for receiving one of said first and second external complementary clock signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

23. (Amended) The circuit of claim 16, further comprising a first and second driver circuit [for boosting said output signal], said first and second driver circuit connected to said first and second complementary clock signal input/output lines, respectively.

26. (Amended) A circuit for reducing signal skew comprising:

at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals;

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second, complementary clock signal input/output line; and

a first and second driver circuit [for boosting said output signal], said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

33. (Amended) The circuit of claim 26, further comprising first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line.

34. (Twice Amended) The circuit of claim 33, wherein each of said first and second input buffer circuits comprises:

an input for receiving one of said first and second external complementary clock signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

87. (Amended) The method of claim 82,[,] wherein said act of receiving first and second external clock signals is performed in connection with the operation of a random access memory.